IR Leds to be rotated in one plane. This allows a degree of freedom of movement for the module to be aligned during installation.

According to a preferred form the mounting is such that it is possible to mount the DVC at any angle on (for example, but not restricted to) a wall, a ceiling, or an adjustable bracket that allows the camera to be easily pointed at an appropriate view. The standard combination of a wide-angle lens and having the image capture assembly internally mounted at a 45° angle means that in most cases the DVC can simply be placed at a location without any internal adjustment being required. In cases where internal adjustment of the image capture assembly is required, it can be rotated up to 45°.

Installing the DVC according to a preferred form involves a plastic mounting plate. The plate is affixed to a wall, ceiling, pan/tilt mount or other camera mount and provides terminals for attaching external wiring for power and Local BUS communications. These wires protrude through the centre of the mounting bracket which is fixed in place with screws. The main DVC enclosure is pushed onto the plastic plate and rotated until it is locked in place. This simultaneously connects the external power and communications terminals through to the electronics within the enclosure by using studs that wipe over a flexible portion of the terminals. A spring-like action ensures good contact between the terminals and the studs.

Throughout the DVC extensive use is made of two discrete logic families. The DVC uses two different supply rails for digital, electronics, namely, 3.3V and 5V. Because of this mixed supply arrangement one of the logic families must be able to interface between the different operating levels effectively.

One of the logic families used is a standard advance CMOS logic series, 74Acxxx. Such devices can be powered by either the 3.3V power rail or the 5V power rail but devices powered by the 3.3V rail cannot be driven by devices powered by the 5V rail. This family is selected as high speed logic is necessary in the DVC and only small propagation delays can be tolerated in many area. The 74Acxxx series is effective and is also readily available.

Another logic family used is the 74LCXxxx family which is specifically designed to be powered between 2.0V and 3.6V. These fast devices with small propagation delays have 5V tolerant inputs. Because the inputs can tolerate 5V signals these devices are particularly used where voltage level-conversion can be a problem.

To more fully describe the construction and operation of the DVC reference will now be made to the camera software operation and design.

As mentioned above, the DVC has three on-board microprocessors each of which performs a different function. While the same functionality could be achieved using one microprocessor this would complicate hardware and software design. As disclosed above, the three processors are a micro-controller in the image capture block 12, the dsp in the main processing block 11 and a micro-controller in the communications block 10 for communications and controlling the down-loadable code.

The major components of the image capture micro-controller PIC code are a frame controller and an asynchronous serial communications to I^2C communications converter.

Referring to Figure 2 the frame controller controls multiplexing of the image capture memory and banking of this memory.

Because the video memory can be accessed by the dsp 17 or the sensor 18 it is necessary to ensure that no accesses take place while the multiplexer 20 is switched to the wrong device. This is accomplished by using a token that is passed back and forth over the token interrupt lines 21 between the image capture controller 19 and the dsp 17. When the dsp 17 has the token the controller 19 switches the video memory to the dsp. When the dsp is finished with the imaging memory it returns the token to the controller 19. The controller 19 then waits until the next frame is due to be read out before switching the memory to the sensor 18. The sensor writes the frame and when it is finished the controller 19 sends the token back to the dsp.

The frame controller module on the controller 19 has several modes to put the image into the video memory in different ways. The first way (default) is to simply put the image into bank B1 all the time. The second mode puts the image into bank B2 all the time. The third alternates the image between the two banks B1 and B2. The final mode captures two images in quick succession and puts them into bank B1 and B2.

The frame controller functionality could be implemented entirely in hardware.

To enable access to all the functionality and configuration control registers of the image sensor 18 a serial communications link is employed. In the preferred form the serial communication standard and protocol used (inter-integrated circuit – I^2C) is not available as a hardware port on the dsp 17. To communicate with this